Docket No. ~~14615~~ 14651

UNITED STATES PATENT AND TRADEMARK OFFICE

VERIFICATION OF A TRANSLATION

I, the below named translator, hereby declare that:

My name and post office address are as stated below;

That I am knowledgeable in the English language and in the Japanese language, and that I believe the English translation of the marked portion of the attached Japanese document is true and complete.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: November 19, 2002

Full name of the translator: Sandra Jayne PARSONS

Signature of translator :

For and on behalf of RWS Group plc

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Notes (see list of cited documents, etc.)

Claims: 1 to 3

Cited document: 1

Remarks:

Cited document 1 (claim 1, [0037] to [0050] of the detailed description of the invention and figures 5, 6 and 7) discloses the sequential writing of correlation values to a memory which respectively collates and stores the abovementioned correlation values of each path in 2 time slots, and, when the correlation values for one time slot have been housed in memory, the collation of the correlation values of said one time slot and the outputting thereof to a RAKE part by the memory part; the invention pertaining to claims 1 to 3 of the subject application is substantially identical to the invention disclosed in cited document 1.

Claim: 4

Cited document: 1

Remarks:

Cited document 1 ([0046] of the detailed description of the invention and figure 6) discloses the sequential housing in memory of the correlation values for each symbol in the order of path 1, path 2, path 3, moving from the lower rank address to the higher rank address, and this corresponds to "when the treatment timing of each finger treatment circuit is

simultaneous, the writing, in accordance with the preferential order determined in advance, of the inverse spread data thereof to the storage circuit" of the invention of claim 4 of the subject application; there is no particular difference between the invention pertaining to claim 4 of the subject application and the invention disclosed in cited document 1, and they are recognized as being substantially identical.

Claim: 5

Cited document: 1

Remarks:

In a comparison of the invention pertaining to claim 5 of the subject application and the invention disclosed in cited document 1, the two differ in that in the invention pertaining to claim 5 of the subject application "the address generated when writing data … (omitted text) … decided on the basis of variables which take the values 0, 1 alternately", whereas there is no disclosure in the invention of cited document 1 relating to variables taking the values 0, 1 alternately in order to determine the address, but as simultaneously performing data writing and reading-out by dividing the memory into 2 memory banks and housing the data blocks alternately in each bank is nothing more than a common means, no novel effect can be recognized in this point (for example, [0045] and

[0046] of Japanese unexamined patent application publication H11-187342, [0064] of Japanese unexamined patent application publication H9-73781, [claim 1] of Japanese unexamined patent application publication H8-194641, and [0083] to [0085] and figure 9 of Japanese unexamined patent application publication H11-203196).

Accordingly, there is no particular difference between the invention pertaining to claim 5 of the subject application and the invention disclosed in cited document 1, and they are recognized as being substantially identical.

Notification will be given should new reasons for refusal be found.

List of cited documents, etc.

1. Japanese unexamined patent application publication 2001-345737

Record of the results of the prior art document search

- Field searched

  IPC edition 7 H04J 13/00 - 13/06

  H04B 1/69 - 1/713

- Prior art documents

  Japanese unexamined patent application publication

H11-331124 (reading out the reception symbol of each path according to identical relative read-out addresses from FIFO to perform synthesis without phase shift when there is a path delay difference across several symbols)

This record of the results of the prior art document search is not a component of the reasons for refusal.